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NANOSIZE VERTICAL TRANSISTOR USING CARBON NANOTUBE AND METHOD OF MANUFACTURING THE TRANSISTOR

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Abstract of JP 2002110977 (A)

PROBLEM TO BE SOLVED: To provide a nanosize vertical transistor using carbon nanotubes which can be integrated at a high degree of integration in a tera-bit scale, and to provide a method of manufacturing the transistor. SOLUTION: Holes, 10', having diameters of several nm, are made through an insulating film 10 of alumina, etc., formed on a substrate and carbon nanotubes 100 are formed by at least one method selected from a chemical vapor phase film forming method, an electrophoresis method, and a mechanical method and arranged vertically in the holes 10' as channels. In addition, gate electrodes 20 are formed near the peripheries of the nanotubes 100, by using the conventional semiconductor device manufacturing method and, at the same time, thin nonconductor films 30 are formed on the gate electrodes 20 so as to bury the holes 10' and source electrodes 40 and drain electrodes 50 are respectively formed on and under the nanotubes 100. Consequently, the nanosize vertical transistor, which has a vertical structure of a tera-bit scale, operates with little power consumption, and uses the carbon nanotubes 100, is obtained.